

Radio Astronomy FX Correlator on Reconfigurable Hardware

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Introduction

In order to improve sensitivity, telescopes require additional collecting area. Instead of using a single, large dish which is expensive to construct and complicated to maneuver, modern radio telescopes use an array of smaller dishes. The signals from these are processed in real-time in order for the multiple dishes to appear to astronomers as if the signal was received from a single dish (beam forming). It also allows a larger area of the sky to be viewed simultaneously. This arrangement is cheaper, more flexible and simpler to construct.

However, it requires that the antennas' signals be summed together to form a coherent picture of the sky. This process is called correlation and involves multiplying each antenna's signal with every other antenna's. The complexity of this calculation scales with the number of antennas squared. Furthermore, it is a difficult signal routing problem.

Traditionally, the solution has been complicated, using custom application-specific ICs. This project aims to use reconfigurable hardware and commercial, off the shelf network switches to perform the same function. Furthermore, we aim to simplify and reduce typical development time of a correlator from 10 years to one year.

These goals are in line with the University of California, Berkeley's Center for Astronomy Signal Processing and Electronics Research (CASPER) group. In a collaborative arrangement, I will continue the work of Aaron Parsons in developing these packetized correlators.

Goals

Produce a working, ready-to-deploy, 32 antenna correlator with 200MHz bandwidth and 2048 channel FFT by the end of 2008.

Deploy a correlator in the field.

Obtain integration periods in the order of 1 second.

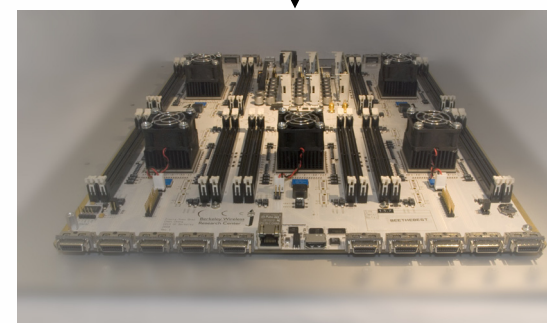
Progress to date

Successfully compiled a 32 antenna correlator with 2k channels and 150MHz bandwidth onto 16 IBOBs and 4 BEEs using a 16 port switch.

Verification is currently underway

Integration times are currently ~16 seconds.

Signal Flow And Hardware



Antennas

The signals from multiple high bandwidth dishes are amplified and routed directly to the digitizers.

IBOBs

Internet Break-out Boards

- High performance 2GSa/s digitizers
- 200Mhz band extracted digitally
- Filtering and 2048 channel FFT
- Data is reformatted for Ethernet network

10Gbps Ethernet Switches

- Commercial, off-the-shelf switches
- Currently CX-4 connectors
- Viable 10G base-T coming soon

BEE2s

Berkeley Emulation Engines

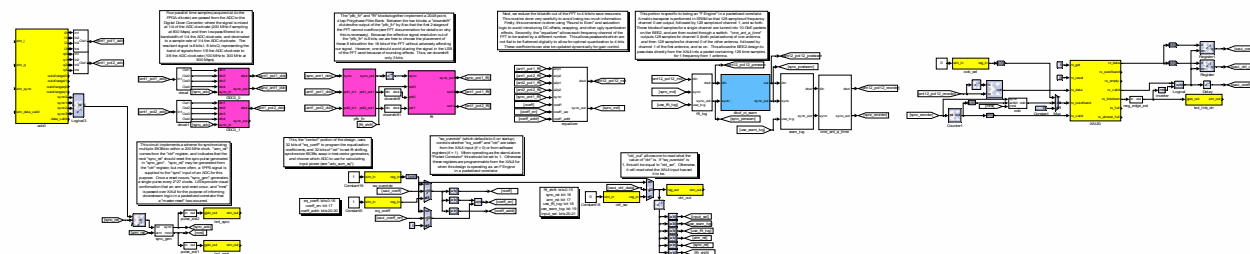
- Performs correlations of all baselines
- Integrates data
- Outputs over standard Ethernet

Software and Firmware

Existing software and scripts originally written by Aaron Parsons in Python are being rewritten in C in order to increase system performance.

The firmware programming language makes use of CASPER's open-source MATLAB Simulink library for IBOB and BEE boards. It is a graphical language that compiles logic operations on data streams into FPGA firmware.

Below is an excerpt from the IBOB design in Simulink.



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