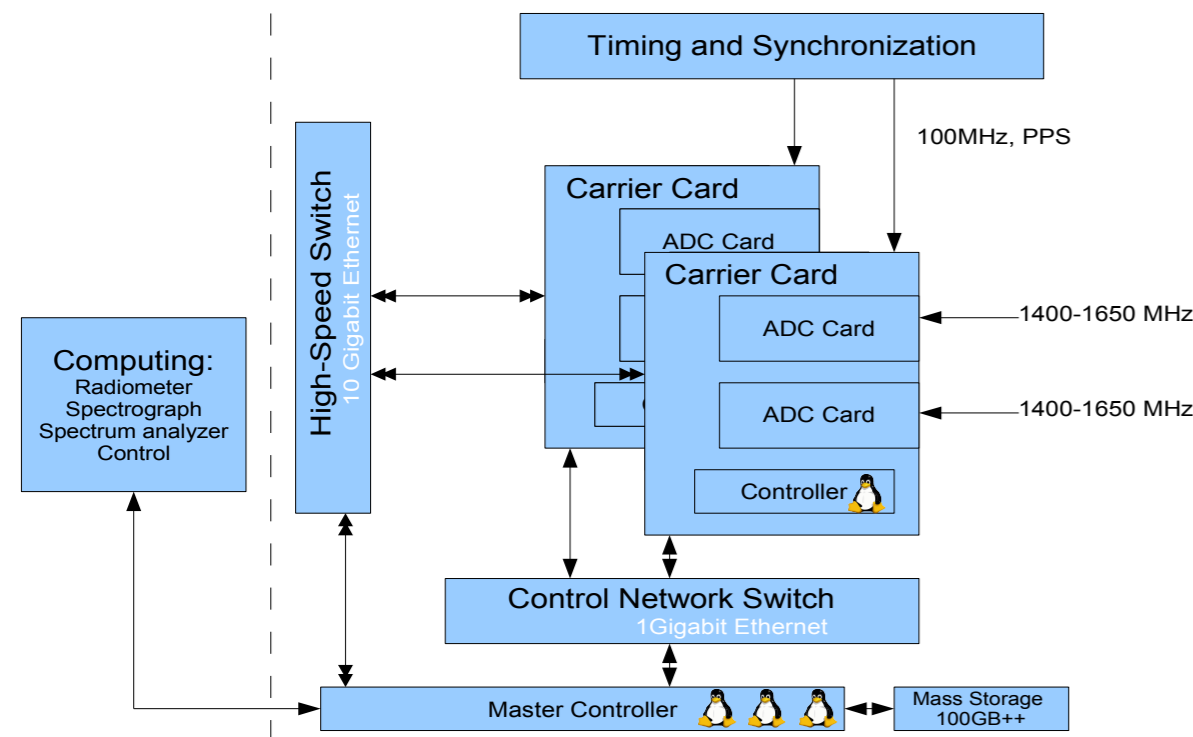# The Design and Implementation of a Carrier Card for the Karoo Array Telescope

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KAT Prototype: XDM Digital Back-End Plan A

- Input Signal: 1400-1650Mhz

- Sample and processed with ADC Cards

- ADC Cards plug into the **Carrier Card**

- This project involves the design and development of the **XDM Carrier Card [XCC]** design

- Carrier Card Transmits processed data via Ten Gigabit Ethernet

XCC Requirements

- Include 2x 10 Gigabit Ethernet link

- Support up to 4GB DDR2 Memory

- Include Reconfigurable Logic to operate memory, communications and perform processing

- Include Controller Capable of running Linux

- Implement System Health Monitoring

XCC Key Features

- 2 x Xilinx Virtex-4 FX60 FPGAs

    - Includes support for direct Implementation of 10Ge

- 2 x DDR2 SODIMMs

- FX12/PowerPC -based computer-on-module

- Actel Fusion AFS600 Mixed-signal FPGA

    - include ADC for measuring voltages/current/temperatures

XCC Key Deliverables

- XCC Schematics

- XCC Layout [Contracted]

- Gateware for Fusion FPGA

- Gateware for FX60 FPGAs

- XCC related Gateware for Controller FX12

- Integrated and Tested System

Primary References

- *Handbook of Digital Techniques for High-Speed Design*, Tom Granberg

- *High-Speed Digital Design: A Handbook of Black Magic*, Howard Johnson & Martin Graham

- Numerous Data-sheets

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