## STUDENT NUMBER:

PLEASE ANSWER IN SPACE PROVIDED OR ON SEPARATE PAGE
MAKE SURE YOUR STUDENT NUMBER IS ON YOUR ANSWER PAGE(s) TOTAL NUMBER OF QUESTIONS : SIX
time(min):

| \# | Question | Marks |
| :---: | :---: | :---: |
| Q1 | Briefly explain what is meant by the concept of 'configuration architecture'. | 5 |
|  |  |  |
| Q2 | What does the Z in Z-RAM stand for? (circle the correct option below) <br> (a) zero-latency <br> (b) zero-power <br> (c) zero-resitors <br> (d) zero-capacitor <br> (e) zero-current | 2 |
| Q3 | FLASH has the problem of memory wear. After what number of erase/write cycles do commercial flash memory tend to start breaking down and loosing data? <br> (a) 10,000,000 cycles <br> (b) 1,000,000 cycles <br> (c) 100,000 cycles <br> (d) 10,000 cycles <br> (e) 1,000 cycles | 2 |
| Q4 | Briefly explain the difference between a latch and a flip-flop [3 marks]. Which one of these has the characteristic of transparency? [1 mark]. | 4 |
| Q5 | Briefly explain the difference between Xilinx SLICEM and SLIDEL configurable logic blocks (CLBs) that they used in many of their Vertex FPGA designs [3 marks]. Motivate why it is often better to have a FPGA structure like this one (i.e. with different types of CLBs) instead of having all the same CLBs [2 marks]. | 5 |
|  |  |  |
| Q6 | Refer to the diagram overleaf and complete the questions that follow. As indicated at the top of the next page, you need to complete the parts of the drawing indicated by the large arrows. You need to indicate how the FPGA would be configured to store the following VHDL statement: <br> 01 <= ( $\mathbf{I 1}$ AND I2) OR I6; Note that I1, I2, I6 correspond to the inputs shown on the left side of the diagram, while O1 corresponds to one of the outputs shown on the right side of the diagram. The Flip Flops (FFs) on the top left of the figure are used to configure the input muxes (each input MUX directs one of four input options to its output). | 12 |
|  | TOTAL | 30 |



