EEE4084F Quiz 2: Lectures 5-12; CH 9, 10, 13

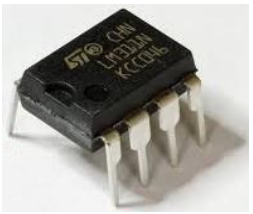
16-Apr-13

This quiz is for marks! Maximum recordable mark is 100%.

PLEASE ANSWER ON A SEPARATE PAGE / IN ANSWER BOOKLET

MAKE SURE YOUR STUDENT NUMBER IS ON YOUR ANSWER BOOK

TOTAL NUMBER OF QUESTIONS : EIGHT

#	Question	Marks
Q1	Provide a rough block diagram illustrating the design of a Von Neumann computer architecture. Label the blocks appropriately; you need not provide a written explanation.	5
Q2	Flynn's taxonomy is used to differentiate between four general designs of computer system. What is the name, and the respective acronym, for each of the four types of computer system in Flynn's taxonomy?	4
Q3	(a) Explain the difference between uniform memory access and non-uniform memory access. [2 marks] (b) Motivate uniform memory access would be more applicable for use in the design of a SMP computer architecture [4 marks]. (c) What is a major disadvantage of using a shared memory design? [2 marks]	8
Q4	These multiplechoice questions relate to CH9 and CH10 of the textbook: (a) Performance of an HDL fabricated ASIC chip is roughly speaking how much faster/slower than running the same design on an FPGA? Choose one option below: (i) 1/100 the speed (ii) 1/10 the speed (iii) 1x i.e. same speed (iv) 10x or more [2 marks] (b) Consider the image on right. Select one of the options i - iv to indicate what this type of chip package is called: (i) PGA (ii) DIL (iii) BGA (iv) MPA [2 marks]  (c) Answer either True of False to each of these questions: (i) A MOSFET occupies a smaller area than a BJT (ii) BiCMOS comprises two CMOS circuits joined together (iii) CMOS tends to dissipate more power than a classic bipolar transistor circuit [1 mark each => 3 marks] (d) Xilinx FPGA are made up of interconnects and two other basic building blocks. Select one answer below that indicates the other two building blocks of a Xilinx FPGA: (i) BIO, CLB (ii) CLB, IOB (iii) BOI, BLC, (iv) CLB, OIB [2 marks]	9
Q5	Explain the difference between static and dynamic CMOS logic. [4 marks] Use a diagram to aid your explanation. [4 marks] Indicate which one of these design approaches tends to operate more quickly than the other. [2 marks]	10
Q6	Consider the image processing operation of blurring for the following questions: (a) Functional decomposition and domain decomposition are two different methods to partition a problem into parts. Explain the difference between functional and domain decomposition. [4 marks]. (b) Motivate why it is likely more effectively to use domain decomposition rather than functional decomposition to parallelize an image blur opertation. [2 marks] (c) If an 3x3 image blur were applied to a highres image, would this be classified as a problem exhibiting coarse grained or fine grained granuality? [2 marks]	8

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Q7	Answer the following: (a) Define bandwidth. [2 marks] (b) Is the visibility of communications for the message passing programming model considered poorly visible or highly visible? [2 marks] (c) Commonly used collective comminication models include the 'reduce' and the 'gather' techniques. Explain the difference between these two techniques (you can include a rough diagram if you like). [4 marks]	8
Q8	Answer the following: (a) What is meant by 'barrier synchronization'? [2 marks] (b) What does the development activity of 'load balancing' involve? [2 marks] (c) Name two types of commonly used design patterns. [2 marks] (d) What is the difference between the development processes of 'vefication' and 'validation'? [2 marks]	8
	TOTAL :	60